2012

U2U

USER2USER

- EUROPE -

The Conference for Mentor Graphics User.

This highly interactive, in-depth technical conference will focus on the needs of the entire Mentor Graphics user community. Attendees will share with their colleagues their best practices, experiences, and challenges together with the tips and tricks that they have learned about how to use Mentor tools in designing, developing and deploying leading edge products.

Park Hilton | Munich, Germany

October 25th, 2012

- IC Manufacturing
- FPGA /ASIC Design
- IC Design
- PCB Design

Mentor Graphics®

General Information

2012 U2U USER2USER - EUROPE -

Don't miss your opportunity to:

- Discover case studies from Mentor Graphics customers all around Europe
- Take part in discussions concerning Mentor Graphics Solutions
- Learn about technology news and design solutions including IC Manufacturing, FPGA /ASIC Design, IC Design and PCB Design (PCB sessions offered in both German and English)
- Take advantage of great networking opportunities
- Visit our Exhibition area and attend the get-together event at the end of the day

Topics covered:

The topics covered, in addition to industry Keynotes, will include IC Design; IC Verification; Functional Verification of digital designs; and PCB System Design (in both English and German Language).

Networking

Don't miss the exclusive networking event – the perfect place to build lasting relationships through face-to-face connections.

Directly after the conference you will have the opportunity to mingle with your peers.

The exclusive networking event with music, finger food buffet and cocktails will take place at the Hilton Restaurant Marco Polo; enjoy spectacular views on the 15th floor!

Conference Hotel

Hilton Munich Park

Am Tucherpark 7

80538 Munich, Germany

Phone +49 89 384500

Keynotes

Organizing by Design

9:20am - 9:50am

Wesley Ryder | Worldwide Technical Director | Mentor Graphics

Winning products are rarely the result of optimizing only one aspect of a design. Innovators generate success because they find ways to cross organizational and functional boundaries to optimize a product in multiple disciplines. Mature companies try to solve this problem by creating cross-disciplinary teams while startup companies do it naturally due to lack of enough resources to allow specialization. Meanwhile, products targeted at customers in different disciplines rarely appeal to more than one. Wes Ryder has compiled data on cross-disciplinary product successes including attempts by companies to create products for hardware/software co-design, mechanical/electrical design integration and many more. He has identified successes and categorized the ways that companies have (rarely) achieved multi-disciplinary product optimization. He will use these examples to generate some guidelines for companies of all sizes to achieve product development success.

Development in a Leading Market

9:50am - 10:20am

Matthias Voigt | General Manager Engineering Group | Renesas Electronics Europe

The progress of industry, generating competitive solutions for a global market will be illustrated. Highly dynamic market segments and related solution-making will be discussed. Examples of our electronics industry will be reflected for Europe.

Agenda - October 25th, 2012 - Park Hilton, Munich, Germany

08:00 - 09:20	**Registration & Welcome & Breakfast**				
09:20 - 09:50	**Keynote: Organizing by Design** - *Wes Ryder, Technical Director, Mentor Graphics* - *Room: Ballroom*				
09:50 - 10:20	**Keynote: Development in a Leading Market** - *Matthias Voigt, General Manager Engineering Group, Renesas Electronics Europe* - *Room: Ballroom*				
10:20 - 10:50	**Coffee Break**				
	IC (CALIBRE) Track	**IC DESIGN Track**	**FUNCTIONAL VERIFICATION Track**	**PCB DESIGN Track** *(German Language)*	**PCB DESIGN Track** *(English Language)*
	Room: Salon van Gogh	*Room: Salon Picasso & Dali*	*Room: Salon Rumford*	*Room: Ballroom B+C*	*Room: Ballroom A*
10:50 - 11:40	**What You Need to Know to Design at 20nm! - Calibre Roadmap Update** *Mentor Graphics*	**IC Update** *Mentor Graphics*	**Transforming Verification Revenge of the Respin** *Mentor Graphics*	**Integrated Systems Design for Industries in Transition** *English language* *Mentor Graphics*	
11:40 - 12:20	**A Novel Approach to Dummy Fill for Analog Designs Using Calibre® SmartFill™** *Cambridge Silicon Radio, UK*	**Scan Test Compression Access for Diagnosis in Application** *NXP Semiconductor, France*	**Digital to Mixed-Signal Verification of Power Management SOCs using Questa-ADMS** *ST-Ericsson, France*	**Expedition PCB & HyperLynx – ZWEI Design Flows integriert in EINEM Entwicklungsprozess** *Harman, Germany*	**Building a Competitive Edge through Performance Excellence** *Guy Brill, Management Consultant, Israel*
12:20 - 13:40	**Lunch**				
13:40 - 14:20	**Fully Integrated Litho Aware PnR Design Solution** *STMicroelectronics, France*	**Effects of Various EDT Channels Allocations on Test Cost and Quality on a 40nm Testcase** *Broadcom, Israel*	**Functional Safety Features in ARM Cortex-R processors** *ARM, UK*	**Der DRC - ein oft unterschätztes Prüfmodul im PCB-Designprozess** *GCD Print Layout, Erlangen*	**PCB Design Process Excellence: Applied within a Transnational, Multi Cultural Organisation** *EADS Astrium, UK*
14:20 - 15:00	**Automated Flow for Voltage Dependent Layout Checks** *Infineon, Romania*	**Implementing a 256 Processor Array Core Using Olympus-SoC** *Kalray, France*	**OVM Adoption: Is It Worth It? Flashback on 4 Years of OVM Adoption** *ST-Ericsson, Germany*	**Trivialität Leiterplatte - Träume werden wahr** *Diehl BGT Defence GmbH & Co. KG, Germany*	**On the Way to Hierarchical Design** *Fujitsu Technology Solutions, Germany*
15:00 - 15:40	**Calibre Auto Waiver in TowerJazz DRC Flow** *TowerJazz, Israel*	**Using Olympus-SOC in Advanced 28nm Designs with Sondrel's Neon and Helium** *Sondrel, UK*	**Formal Verification of an Interrupt Controller** *Infineon, Germany*	**Präsentation der Mentor Graphics UserGroup** *Mentor UserGroup, Germany*	**MECODES EDMD Solution for Collaboration between Mentor Graphics Expedition Enterprise and CATIA V5** *CADCAM Group, Croatia*
15:40 - 16:30	**Closing & Prize Draw & Exhibition** - *Room: Ballroom*				
16:30 - 19:00	**Get together** - *Restaurant Marco Polo, 15th floor*				

Technical Session Highlights

IC (Calibre) Abstracts

What You Need to Know to Design at 20nm! - Calibre Roadmap Update | 10:50am - 11:40am

David Abercrombie | Program Manager, Advanced Verification Methodology | Mentor Graphics

Double Patterning, TSV's, DRC+, advanced extraction rules are all new things that a designer needs to consider at 20nm. And, oh yeah, they need to be addressed within the existing design flow for fast adoption and use, since designers still need to deliver the chip in time for Christmas! Are the Mayans right about this being the end of the world, or is it just another Y2K panic attack? Come learn about the issues you are experiencing and what Calibre is doing to help.

A Novel Approach to Dummy Fill for Analog Designs Using Calibre® SmartFillTM | 11:40am - 12:20pm

Colin Thomas | Cambridge Silicon Radio LTD

With small geometry silicon processes, additional nonfunctional geometric structures are required to maintain layer planarity during the Chemical Mechanical Polishing (CMP) phase of processing. The automated layout flows to generate such geometries tend to be designed primarily for large System On a Chip (SOC) digital designs. When applied to mixed signal layout these have been seen to have issues in both delivering the required layer densities, and with flexibility in maintaining symmetry for device matching. In this paper, we describe a novel approach where the dummy patterns can be easily customised and controlled from a design entry system, and used to drive a Tcl programmable Calibre® SmartFillTM engine to allow the flexibility required to add dummy fill to a variety of analog layout styles.

Fully integrated litho aware PnR design solution | 1:40pm – 2:20pm

Fabrice Bernard-Granger | DFM CAD Solutions Engineer | STMicroelectronics, Crolles, France

Design For Manufacturing (DFM) is becoming essential to ensure good yield for deep sub micron technologies. As design rules cannot anticipate all manufacturing marginalities resulting from problematic 2D patterns, the latter has to be addressed at design level through DFM tools. To deploy DFM strategy on back end levels, STMicroelectronics has implemented a CAD solution for lithographichotspots search and repair. This allows the detection and the correction, at the routing step, of hotspots derived from lithographic simulation after OPC treatment. The detection of hotspots is based on pattern matching and the repair uses local reroute ability already implemented in Place and Route (PnR) tools. This solution is packaged in a Fast LFD Kit for 28 nm technology and fully integrated in PnR platforms. It offers a solution for multi suppliers CAD vendors routed designs. To ensure a litho friendly repair, the flow integrates a step of local simulation of the rerouted zones. This paper explains the hotspots identification, their detection through pattern matching and repair in the PnR platform. Run time, efficiency rate, timing and RC parasitic impacts are also analyzed.

Automated Flow for Voltage Dependent Layout Checks | 2:20pm - 3:00pm

Radu Stoica | Infineon, Bucharest, Romania

Integrated circuits with power devices can contain domains with high operating voltages. In these circuits, special design rules like extended spacings need to be applied between shapes with large potential differences. So far it has been very difficult to predict the relevant voltages and use them as parameters for layout verification checks. As a consequence, conservative verification approaches have led to unnecessary silicon space requirements. We present a seamless verification flow, which requires from the user as the only input the expected voltage ranges for the ports of the design. To ease the debugging the error markers are attributed with schematic net names and the predicted voltages.

Technical Session Highlights

Calibre Auto Waiver in TowerJazz DRC Flow | 3:00pm - 3:40pm

Oren Amir | Senior Program Manager | Mask Technology Group TowerJazz, Israel

Waivers in PV (Physical Verification) refer to DRC violation that has been approved by the wafer manufacturing not to be fixed. Mostly, all DRC violations MUST be fixed before mask manufacturing. In today's design, the use of IP (intellectual property) is increasing therefor the number of waivers that the designer has to deal with is increasing, also. There are many approaches on "How to deal" with waivers, from the most strict one which says each DRC violation MUST be inspected, to the most loose one that say don't look in violations if the violation name is the same as the waiver name (e.g. poly space). Each approach has its own gain and risk, starting with the strictest one that the gain will be of no risk at all (risk = true DRC violation) but consuming a lot of debug time, or the most loose approach that costs minimum time consuming but with high risk. In our work we used the new waiver approach, from Mentor Graphics, which shows combination of no risk with minimum time in debugging waivers. We will present our old approach (e.g. flow) of dealing with a waiver and the new flow with Calibre auto waiver. We will present some design data, including run time, and a number of drc violation and the number of waivers that we have to deal with.

IC Design Abstracts

IC Design Product Update | 10:50am - 11:40pm

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Scan Test Compression Access for Diagnosis in Application | 11:40am - 12:20pm

Paul-Henri Pugliesi-Conti | DFT & Test Architect, BU Identification / NXP Semiconductor Caen, France

Although techniques are available to ensure a standard test access at System-in-Package (SiP) or System level, the issues related to in-situ-testing are not addressed in DFT solutions so far, because of many factors (lack of, or poor controllability and observability of dynamic signals, long access time for solution based on JTAG access only, large silicon overhead for solution based on BIST). In this work, author has developed a novel generic solution for testing Stuck-At and Transition faults on an embedded IC (in a system/SiP) through only a standard JTAG interface. The solution is be based on the use of new Mentor-Graphics Testkompress capabilities and reuse of the JTAG interface architecture.

Effects of Various EDT Channels Allocations on Test Cost and Quality on a 40nm Testcase | 1:40pm - 2:20pm

Arik Krantz / DFT Engineer / Broadcom Corporation, Israel

One of the paramount decisions during the design process is test pads allocation. The amount of available test pads and their allocation can directly impact the test quality and cost. With increased design complexity and reliance on scan compression techniques, it is imperative to optimize compression channels allocation. Previous TK benchmarking results have shown the potential benefits of using asymmetric allocation of compression channels over a traditional, symmetric one. In those cases, an improvement in pattern count and effective compression was typically achieved by allocating a larger amount of input channels, compared to output channels. [ADD reference]. In this paper we will present an evaluation of various asymmetric channel allocations on an advanced 40nm testcase, where following the path of increasing input channels actually degrades the compression effectiveness. We will review the reasons for it, and find a more optimal allocation, which may be applicable to other designs.

Technical Session Highlights

Implementing a 256 Processor Array Core Using Olympus-SoC | 2:20pm - 3:00pm

Francois Jacquet | Head of Physical Design / Kalray, France

Transitioning to 28nm has been a big challenge for designers due to various design complexities. Increasing design sizes, high performance targets, low power needs (advanced Multi-Voltage) and increasing DRC/DFM rule count have a huge impact on project cycle time and quality of results. In this session I will talk about a processor array core netlist to gdsii implementation at 28nm using Olympus-SoC, and how these design challenges were addressed effectively. Advanced Multi-VDD flow including complex PST, Multi Corner, Multi-Mode optimization and DRC/DFM sign-off during implementation will also be covered.

Using Olympus-SOC in advanced 28nm designs with Sondrel's Neon and Helium | 3:00pm - 3:40pm

Sub Johal | Sondrel, UK

The detailed P&R design of an Advanced multi-core 28nm HD Video processor is presented. The presentation will show how key and unique features provided in Olympus-SOC such as virtual flat design, multi-mode multi-corner optimisation, full UPF support, hyper-threaded tooling and in-tool signoff quality DRC fixing with Calibre-inRoute have allowed the predictable and timely implementation of extreme complexity. Two unique products which are used by Sondrel to de-risk and enable the design cycle, namely Neon and Helium will also be presented. With Neon, the management processes and procedures are captured in protocols, which define the evolution of a design from initial "Discovery" to final "Finishing". The Helium flow provides the automated wrapper which drives tools like Olympus-SOC, FormalPro, Calibre and sign-off tools, and captures the best-practice collected from the many successful Sondrel tapeouts completed and many thousands of engineer hours on real P&R tasks. This flow is unique in that it has been developed and enhanced by the actual engineers on this project and many other designs.

Functional Verification Abstracts

Transforming Verification: Revenge of the Respin | 10:50am - 11:40pm

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Phones are becoming computers. Cars are changing into self-navigating mobile offices. TVs are morphing into 3-D Everything On-Demand Entertainment and Information consoles. Your products are transforming, some even on-the-fly after you deliver them. So why aren't your verification practices transforming as well? This year we will take a focused look at three vital solutions that will not only help you defend the universe against the dreaded Respins (and possibly save your job), but are actually easy to deploy in a matter of days. Leave your manager at the office so you can take all the credit for finding these ways to make you and your verification „more than meets the eye."

Technical Session Highlights

Digital to Mixed-Signal Verification of Power Management SOCs using Questa-ADMS | 11:40am - 12:20pm

Mathieu Behaghel | ST-Ericsson, Grenoble, France

AMS and RF designs done in ST-Ericsson have big analog functionalities and a lot of interaction between analog and digital functionalities. The partitioning of these designs makes them particularly difficult to verify. The most accurate solution would be to simulate the complete design with a spice simulator, however, increasing time to market constraints and circuit complexity make this approach impossible.

As ST-Ericsson is a platform company, models have to be compatible with pure digital tools to simulate all the SOCs platform together. As a consequence, we decided to use a digital centric methodology with real numbers to model the analog functionality. This presentation will show how we developed the models to verify most of the design connectivity and functionality using the speed of digital simulators. It will then describe how Questa-ADMS was used to cover the electrical behavior of the design by reusing the digital on top environment. Examples will be taken from a power management SOC.

Functional safety features in ARM Cortex-R processors | 1:40pm - 2:20pm

Christopher B. Turner | ARM Ltd., Cambridge, UK

This presentation will describe the latest ARM Cortex-R high performance embedded processors and introduce their features which relate to functional safety. These features enable the design of microcontroller devices for use in systems requiring high reliability and high availability for integrated control and safety applications. The focus will be on the Cortex-R processor's capabilities for error detection and correction, deterministic responsiveness and redundancy. Applications for these processors are in automotive and industrial control and these will be discussed together with system design scenarios for arriving at a suitable Automotive Safety Integrity Level (ASIL) in line with the new ISO26262 standard for functional safety.

OVM Adoption: Is it Worth it? Flashback on 4 years of OVM Adoption | 2:20pm - 3:00pm

Markus Goertz | ST-Ericsson, Nuremberg, Germany

Adopting new technology is by no doubt a challenge as it requires an up-front investment on the first projects with no guarantee of ROI in the long run if not carefully thought through and planned. 4 years ago, we took the step of moving from? To OVM for our verification IP testbenches. If we take a step back and look behind, we have seen how tools have improved in terms of OVM support, the impact it has on our verification cycle and a first estimation of the ROI. In that session we would like to walk you through our journey and present how we build up our ecosystem, the improvements we have seen in terms of OVM support and the impact of adopting OVM.

Formal Verification of an Interrupt Controller | 3:00pm - 3:40pm

Othman Bahlous | Infineon, Munich, Germany

„We describe our efforts to formal verify a real-world interrupt controller design used on an Infineon microcontroller flash memory subsystem. The design under verification does not only have intricate control logic, but it also uses micro-code that is applied as interrupt routines. We use a methodology involving specific steps, including capturing requirements, formulating assertions, and executing a tool. The design behavior is captured by SystemVerilog Assertions (SVA) and run on Questa Formal. Questa Formal was able to catch a logical bug and several design specification ambiguities."

PCB Design Abstracts (German language)

Expedition PCB & HyperLynx – ZWEI Design Flows integriert in EINEM Entwicklungsprozess | 11:40am - 12:20pm

Liviu-Dumitru Craciun | Harman, Germany

Der Vortrag befaßt sich mit der Umsetzung „theoretischer Anforderungen" der Schaltungsentwickler in die reale Welt der Leiterplattenherstellung durch den Leiterplatten-Designer (Layouter). Anhand von Beispielen werden die Auswahlkriterien und Abhängigkeiten die zur Realisierung von komplexen Leiterplatten (mit Mentor Tools) führen, erläutert. Außerdem soll in diesem Vortrag gezeigt werden, daß sich aus dem Beruf des einfachen Layouters, der nur für die Entflechtung von Schaltungen zuständig war, der Beruf des Leiterplatten-Designers entwickelt hat, der zusätzlich zum Layout, die elektrotechnischen Zusammenhänge und die wesentlichen Randbedingungen der Leiterplattenfertigung kennen muß.

Der DRC - ein oft unterschätztes Prüfmodul im PCB-Designprozess | 1:40pm - 2:20pm

Detlef Lehmann | GCD Printlayout GmbH, Erlangen

Um die Zuverlässigkeit und Fertigbarkeit einer Leiterplatte zu erhöhen und den heutigen Anforderungen an ein Layout gerecht zu werden , ist es nötig jedes Layout vor der Freigabe genau zu prüfen , und so zu gestalten, dass eine möglichst günstige Fertigbarkeit entsteht. Ich zeige:

- Wie man bei der Gestaltung des Layouts unter Zuhilfenahme des DRC für die Fertigung der Leiterplatte Kosten sparen kann.
- Wie man die Qualität erhöht durch Differenzierung der Technologietreiber auf der Leiterplatte und Einteilung in Ruleareas.
- Was kann ein DRC abdecken? Was nicht ?

Trivialität Leiterplatte - Träume werden wahr | 2:20pm - 3:00pm

Dieter Wachter | Diehl BGT Defence GmbH & Co. KG, Überlingen, Germany

Der Vortrag befaßt sich mit der Umsetzung „theoretischer Anforderungen" der Schaltungsentwickler in die reale Welt der Leiterplattenherstellung durch den Leiterplatten-Designer (Layouter). Anhand von Beispielen werden die Auswahlkriterien und Abhängigkeiten die zur Realisierung von komplexen Leiterplatten (mit Mentor Tools) führen, erläutert. Außerdem soll in diesem Vortrag gezeigt werden, daß sich aus dem Beruf des einfachen Layouters, der nur für die Entflechtung von Schaltungen zuständig war, der Beruf des Leiterplatten-Designers entwickelt hat, der zusätzlich zum Layout, die elektrotechnischen Zusammenhänge und die wesentlichen Randbedingungen der Leiterplattenfertigung kennen muß.

Präsentation der Mentor Graphics UserGroup | 3:00pm - 3:40pm

Hanno Platz | Leiter der Mentor UserGroup, Germany

Die deutschsprachige Mentor Usergroup ist ein lockerer Zusammenschluss von interessierten Anwendern. Die Leitung erfolgt über Regionalgruppenleiter, in derzeit 6 Regionalgruppen in Deutschland und einer in der Schweiz. Die Regionalgruppen treffen sich jeweils 1-2 im Jahr um fachlichen Wissensaustausch zu betreiben. Der Leiter des deutschsprachigen Forums, Hanno Platz, betreibt eine Webseite unter der Adresse www.mentoruser.org und ein Emailforum bei dem jeder interessierte Mentor-Anwender Mitglied werden kann.

Technical Session Highlights

PCB Design Abstracts (English language)

Integrated Systems Design for Industries in Transition | 10:50am - 11:40am

N.N. | Mentor Graphics

As product complexity has increased, organizations have been under constant pressure to meet their business drivers while bringing competitive products to the market-place. These pressures are being compounded by a significant demographic shift in heritage PCB design and engineering. In the western world, new entrants into the PCB design workplace is in decline, this is happening when engineering graduates as a whole are also in decline. Meanwhile, products are becoming more complex where, what was once isolated processes are now very much integrated. To ensure the viability of the next generation of engineering, there is a drive to lower the barriers to perform core engineering and design activities while enabling organizations to take a systems approach in their development strategies. This keynote will cover these trends and introduce Mentor's view of integrated systems design for an industry in transition by showcasing specific technologies that will enable next generation of PCB development.

Building a Competitive Edge through Performance Excellence | 11:40am - 12:20pm

Guy Brill | Management Consultant | Israel

Engineering tools provided by Mentor as well as some others can be utilized best when implemented in accordance with the company's strategy in order to achieve a competitive edge. The presentation describes how a $2.7 billion defense electronics company developed the approach that guided its implementation of tools and methodologies to achieve performance excellence. The resulting environment served the company in improving the execution of a large variety of projects including design, manufacturing and service of simple as well as complex solutions. The presentation is giving the perspective of the executive VP who led the process of building the multi-disciplinary operational environment and its adaptation following changes in the business environment. The presentation provides a template that can be used by other companies that need to achieve performance excellence as an essential part of their strategy.

PCB Design Process Excellence: Applied Within a Transnational, Multi Cultural Organisation | 1:40pm - 2:20pm

Jon Hill | EADS Astrium, UK

This presentation will highlight Astrium's organisation & culture, it's business drivers and product/design characteristics. It will go on to discuss how this translates into a need for access to improved PCB technology and how Astrium chose to harmonise it's design process around Mentor Graphics Expedition Enterprise flow. The challenges of aligning a multi-cultural organisation will then be discussed with practical examples of actions that led to sharing of best practices and realising a "Design Anywhere Build Anywhere" design environment.

On the Way to Hierarchical Design | 2:20pm - 3:00pm

Andreas Schaefer | Fujitsu Technology Solutions, Germany

In software development we are used to functions, code libraries and object oriented design.But looking onto hardware development, we still haven't done this step, even if our designs would allow to. In this presentation we will show our way towards hierarchical design. We will explain the overall impact to our design flow, the decisions we made, the change in thinking we have to accept. There are still some obstacles and the way is not at is end, but we can show, why it is the right way to go and how the goal could be reached.

MECODES EDMD Solution for Collaboration between Mentor Graphics Expedition Enterprise and CATIA V5 | 3:00pm - 3:40pm

Manfred Sammet | CADCAM Group, Croatia

Electro-mechanical design gains in importance because nearly all products contain both electrical and mechanical systems. Traditionally the design solutions of these two engineering disciplines have their own design methods, data formats and data management systems. As a result, products designed with ECAD and MCAD tools represent the result the non-integrated and domain specific design & process methodologies with limited collaboration between the disciplines. Accordingly, the new MECODES EDMD for CATIA V5 was developed as a unique system for electromechanical collaboration between Mentor Graphics EE and CATIA V5 based on the ProSTEP EDMD recommendations. EDMD is the protocol for ECAD/MCAD collaboration initiated by Mentor Graphics, supported by consortium of vendors worldwide and lead by the ProSTEP iVIP association.

MECODES EDMD Solution consists basically of two integrated subsystems which are essential for a successful collaboration: the Information Repository and the EDMD client for CATIA V5. The core of MECODES Information Repository contains data storage capabilities to enable an efficient collaboration design between the disciplines. The federated MECODES Repository environment provides resources for an integrated design environment. It consists of a linked 3D library for electromechanical components, access control capabilities, collaboration history including restore-to-point functions, a change management tool for real-time collaboration, customer defined attributes like reference designator, creation of value and ID numbers etc. The CATIA V5 EDMD client has implemented the ProSTEP EDMD protocol recommendation v2.1 for collaboration between ECAD/MCAD tools and supports in addition the ODB++ industry standard format for the transfer of enhanced 3D models like cooper layers, wires, silk screen and silk mask. That all results in better productivity, high quality, reduced design cycle times and innovation enabled by the collaborative design across the mechanical and electrical domains.